1754

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#21 6/27/2

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/062,314 02/01/02

S.M. Jang et al.

HARD MASKING METHOD FOR FORMING PATTERNED OXYGEN CONTAINING PLASMA ETCHABLE LAYER

Grp. Art Unit: 1754

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on May 31, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 5/31/02

U.S. Patent 5,700,737 to Yu et al., "PECVD Silicon Nitride for Etch Stop Mask and Ozone TEOS Pattern Sensitivity Elimination," discloses a method for forming dense electrode patterns having a high aspect ratio in a conductor metal layer.

U.S. Patent 5,246,883 to Lin et al., "Semiconductor Contact Via Structure and Method," discloses a method for forming a contact via structure through at least one dielectric layer within an integrated circuit microelectronics fabrication.

U.S. Patent 5,460,693 to Moslehi, "Dry Microlithography Process," discloses a photolithography method for use in fabricating patterned integrated circuit microelectronics layers within integrated circuit microelectronics fabrications, where the photolithography method is undertaken employing dry processing methods only.

U.S. Patent 5,565,384 to Havemann, "Self-Aligned Via Using Low Permittivity Dielectric," discloses a method for forming within an integrated circuit microelectronics fabrication, a self-aligned via through an inorganic dielectric layer to access a patterned conductor layer formed below the inorganic dielectric layer, where the patterned conductor layer has interposed at least partially between its patterns an organic containing dielectric layer.

U.S. Patent 5,654,240 to Lee et al., "Integrated Circuit Fabrication Having Contact Opening," discloses a method for forming a patterned conductor contact layer contacting a semiconductor substrate within an integrated circuit microelectronics fabrication, while avoiding trenching within the semiconductor substrate when etching the patterned conductor contact layer from a corresponding blanket conductor contact layer formed contacting the semiconductor substrate.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761